**Supplements to 51LabWork#1 and #2**

**[1] Discrete LED operations**

(1) Behaviors

|  |
| --- |
| P  Id = IS ( +  where IS : 10-13 ~ 10-19  VT : 25mv at room temperature Id Vd  Id N -    \* when Vd > 0v, the diode is said to be ***forward-biased***,  and Id increases drastically rapid  *ΔI* \* when Vd ≦ 0v, the diode is said to be ***reverse-biased***,  and Id practically non-exists  \* when forward-biased, small *ΔV* variation causes relatively  Vd large *ΔI* swing  IS  \* cut-in voltage Vcut-in of a diode: 0.6-0.7v  *ΔV* ***Vcut-in*** \* ***diode ON*** and ***diode OFF*** |

(2) Intensity control

|  |
| --- |
| Vcc  VH  \* with VH, the LED turns OFF VL \* with VH, the LED turns ON  \* with VL, the LED turns ON \* with VL, the LED turns OFF  \* respective Id values? \* respective Id values?  \* replacing with a 10K resistor? R: 1kΩ \* replacing with a 10K resistor?  R: 1kΩ  VH  VL |

(3) Circuit model of diode

|  |
| --- |
| \* an ***idealized*** diode model Id  - acting like a voltage-controlled when Vd > 0, switch ON  switch  when Vd<= 0, switch OFF  Vd |

|  |
| --- |
| \* a few more somewhat not so idealized diode models  Id Id    rd-1  Vd Vd  VD VD  VD VD  rd |

**[2] Driving and sinking capacity of 51-IOports: P0-P3**

(1)acting as **an output port**

\*driving a pulled-down resistive load \* sinking a pulled-down resistive load

(on) (off)

Pnj: VOH Pnj: VOL

(off) weak (on) virtually

current nil

\*driving a pulled-down LED load \* sinking a pulled-down LED load

(on) (off)

Pnj: VOH Pnj: VOL

LED: deem virtually LED: OFF

(off) (on) nil

\*driving a pulled-up resistive load \* sinking a pulled-up resistive load

(on) virtually  (off)

nil Pnj:VOL

Pnj:VOH

(off) (on) weak

current

\*driving a pulled-up LED load \* sinking a pulled-up LED load

LED: OFF LED: deem

(on) virtually (off)

nil Pnj:VOL

Pnj:VOH

(off) weak

(on) current

\*driving a digital load (Pnj: VOH) \* sinking a digital load (Pnj: VOL)

(on) weak (off) weak

current current

(weak (weak

(off) driving) (on) sinking)

(2)acting as **an input port**

\* receiving a HIGH input: VIO \* receiving a LOW input: VIL

(off) (on)

VOH VOL

(off) ( weak sinking) (virtually nil)

to internal data path to internal data path

**[3] role of the line buffers (also known as line transceivers/line drivers)**

(1) 74244 TTL SSI \* nominal electric ratings

4 x4 4 \* nominal switching rating

\* max/min electric ratings

(e.g., max. of 15ma driving current and 24ma sinking current)

/EN1 \* max/min switching ratings

4 x4 4 \* logic function

/EN2

(2) function of 74244 when 51-IOport outputs LOW: VOL

*WEAK-SOURCE* ***BUFFER*** *HEAVY-LOAD*

Pnj: VOL 244: VOL

much greater sinking current offered [24ma per pin, max.]

51µP with limited

sinking current [1.6ma per port, max.]

**[4] 7-segment LED Operations**

(1) common anode 7-segment LED control

\* circuit diagram a

VCC

f g b

e c

d g

a b c d e f g h \* pattern control?

(2) common cathode 7-segment LED control

\* circuit diagram

a b c d e f g h

\* pattern control?

(3) 7447/7448/7449 TTL SSI: BCD-to-7segment converter [open-collector outputs]

d0 a \* electric ratings (nominal, max., min.)

d1 b \* nominal switching ratings (nominal, max., min.)

d2 c \* overall logic function and pin-assignment

LT e - /LT??

BRI f - /BI??

BI/RBO g - /RBI??

h - /RBO??

- working with common anode/cathode 7-seg LED?



(4) BJTs transistors serving as switches

\* transistors are used as switching devices in digital circuits, and

as amplifying devices in analog circuits;

\* electrical behaviors of BJT(bipolar-junction transistor) in digital ckts: switching between saturation (ON) and cut-off (OFF)

***NPN BJTs***  ***PNP BJTs***

- C [collector] + E[emitter]

Vbc + Veb +

B[base] + Vce B[base] - Vec

+ Ice - Iec

Vbe - Vbc  -

- E[emitter] + C[collector]

-- when Vbe < Vcut-in, I ce 0A; -- when Veb < Vcut-in, I ec 0A;

the transistor, Q, is said to be OFF the transistor, Q, is said to be OFF

-- when Vbe VCC, I ce = Isat and Vce = 0.1-0.2V; -- when Veb VCC, I ec = Isat and Vec = 0.1-0.2V;

the transistor, Q, is said to be ON the transistor, Q, is said to be ON

-- QNPN could thus regraded as a Vbe-controlled switch -- QNPN could thus regraded as a Vbe-controlled switch

C QNPN turned OFF, C-E open-ckt C E QPNP turned OFF, E-C open-ckt E

(logic 0 input) (logic 1 input)

Vbe= VCC Vbe=0 Veb= VCC Veb=0

(logic 1 input) (logic 0 input)

E QNPN turned ON, C-E short-ckt E C QPNP turned ON, E-C short-ckt C

-- ***QPNP***acting as a power-switch for the 7-segment LED module

VCC \*]] when Vin = VCC VCC

Vin ***logic 1*** ***switch-off***,

7-seg LED receiving no pow-supply

\*]] when Vin= 0 VCC

***switch-on,***

7-seg LED receiving power-supply

***logic 0***

-- what if QNPN servining as the power switch?

(5) MOS transistors acting as switching devices in logic gates

\* electrical behaviors of NMOS and PMOS transistors (**enhancement-type**)

***NMOSEN*** (VnTHen > 0V) ***PMOSEN*** (VpTHen < 0V)

VSS

VDD  - S[source]

D[drain] Vgs

G[gate] + G[gate] + +

Vin Vds Vin Vsd

+ - -

Vgs Ids Isd

- S[source]

-- when Vgs > VnTHen, Vds 0V(allowing quite some Ids); -- when Vgs < VpTHen, Vsd 0V(allowing quite some Isd);

QNen is said to be ON QPen is said to be ON

-- when Vgs < VnTHen, Ids 0A (regardless of Vds); -- when Vgs > VpTHen, Isd 0A (regardless of Vsd);

QNen is said to be OFF QPen is said to be OFF

-- QNen thus regarded as a Vgs-controlled switch -- QPen thus regarded as a Vgs-controlled switch

Vin: logic 1[Vgs > VnTHen] Vin: logic 0 [Vgs < VnTHen] Vin: logic 0[Vgs < VpTHen] Vin: logic 1 [Vgs > VpTHen]

D D D D

Vgs Vgs Vgs Vgs

S S S S

\* logic gates by NMOSen

VDD VDD

Vo Vo

Q1 Q2 Q1 Q2 switch status depending on input combinations

Vin1 Vin2

Vin1 Vin2 Q1 Q2 Vo logic

a] when Vin1: logic 1 and Vin2: logic 1 🡪 Q1: ON and Q2: ON 🡪 Vo= 0V VDD VDD on on 0V

b] when Vin1: logic 1 and Vin2: logic 0 🡪 Q1: ON and Q2: OFF 🡪 Vo= 0V 0V VDD off on 0V ?

c] when Vin1: logic 0 and Vin2: logic 1 🡪 Q1: OFF and Q2: ON 🡪 Vo= 0V VDD 0V on off 0V

d] when Vin1: logic 0 and Vin2: logic 0 🡪 Q1: OFF and Q2: OFF 🡪 Vo= 1V 0V 0V off off VDD

Vo Vo Vo Vo

Q1 Q2 Q1 Q2 Q1 Q2 Q1 Q2

VDD VDD

[truth table]

Vo Vin1 Vin2 Q1 Q2 V0 logic

Vin1

Q1 ??

Vin2

Q2

\* logic gates by PMOSen

VDD VDD

Vo Vo

Q1 Q2 Q1 Q2 switch status depending on input combinations

Vin1 Vin2

Vin1 Vin2 Q1 Q2 Vo logic

a] when Vin1: logic 1 and Vin2: logic 1 🡪 Q1: OFF and Q2: OFF 🡪 Vo= VDD VDD VDD off off VDD

b] when Vin1: logic 1 and Vin2: logic 0 🡪 Q1: OFF and Q2: ON 🡪 Vo= 0V 0V VDD on off 0V ?

c] when Vin1: logic 0 and Vin2: logic 1 🡪 Q1: ON and Q2: OFF 🡪 Vo= 0V VDD 0V off on 0V

d] when Vin1: logic 0 and Vin2: logic 0 🡪 Q1: ON and Q2: ON 🡪 Vo= 0V 0V 0V on on 0V

Vo Vo Vo Vo

Q1 Q2 Q1 Q2 Q1 Q2 Q1 Q2

VDD VDD

[truth table]

Vo Vin1 Vin2 Q1 Q2 V0 logic

Q1 0V 0V

Vin1 0V VDD

VDD 0V

VDD VDD

Vin2 Q2

\* electrical behaviors of NMOS and PMOS transistors (depletion-type)

***NMOSdp*** (VnTHdp < 0V) ***PMOSdp*** (VpTHdp > 0V)

VDD  0V

D[drain] - S[source]

Vin switching between Vgs Vin switching between

G[gate] + - VDD and 0V + + VDD and 0V

Vin Vds  G[gate] Vsd

+ - -

Vgs  Ids Isd

- S[source] D[drain]

- VDD

-- when Vgs > VnTHdp, Vds 0V(allowing quite some Ids); -- when Vgs < VpTHdp, Vsd 0V(allowing quite some Isd);

QNdp is said to be ON QPdp is said to be ON

-- when Vgs < VnTHdp, Ids 0A (regardless of Vds); -- when Vgs > VpTHdp, Isd 0A (regardless of Vsd);

QNdp is said to be OFF QPdp is said to be OFF

-- QNdp thus regarded as a Vgs-controlled switch -- QPdp thus regarded as a Vgs-controlled switch

Vin: 0V[Vgs > VnTHdp] Vin: - VDD [Vgs < VnTHdp] Vin: 0V[Vgs < VpTHdp] Vin: VDD [Vgs > VpTHdp]

D D S S

Vgs Vgs Vgs Vgs

S S D D

\* logic gates by NMOSdp ???

VDD VDD

Vo Vo

Vin1 Vin2

Q1 Q2

Q1 Q2

Vin1/2  switching between 0 and –VDD

major difficulty

V0 switching between 0 VDD

Vin1 Vin2 Q1 Q2 Vo logic

a] when Vin1: 0V and Vin2: 0V 🡪 Q1: ON and Q2: ON 🡪 Vo= VDD 0V 0V on on 0V

b] when Vin1: 0V and Vin2: - VDD 🡪 Q1: ON and Q2: OFF 🡪 Vo= 0V 0V - VDD on off 0V ?

c] when Vin1: - VDD and Vin2: 0V 🡪 Q1: OFF and Q2: ON 🡪 Vo= 0V - VDD 0V off on 0V

d] when Vin1: - VDD and Vin2: - VDD 🡪 Q1: OFF and Q2: OFF 🡪 Vo= 0V - VDD - VDD off off VDD

VDD VDD

[truth table]

Vo Vo Vin1 Vin2 Q1 Q2 Vo logic

Vin1 -VDD -VDD VDD

Q1 Q1 0V -VDD VDD

-VDD 0V VDD ???

Vin2 Q2 Q2 0V 0V on on 0V

Vin1/2  switching between 0 and –VDD

major difficulty encountered by the circuit

V0 switching between 0 VDD

**[5] Dot-matrix LED Operations**

(1) circuit diagram

**column control column control power feeding**

c0 c1 c2 c3 c0 c1 c2 c3

VH  VL

OFF ON

r0 r0

r1 r1

r2 r2

r3 r3

\* pattern control?? \* pattern control??

(2) 74373 TTL SSI: line drivers with LATCH

|  |  |  |  |
| --- | --- | --- | --- |
| control | | data path | |
| /OC | LE | IN0-7 | OUT0-7 |
| H | NC | NC | Hi-Z |
| L | L | NC | IN0-7\* |
| H | IN0-7 | IN0-7 |
| [note] IN0-7\*: IN0-7 latched at LE | | | |

IN0-7 OUT0-7

74373

LE

/OC

\* electrical ratings?

\* switching ratings?

(3) 74138 TTL SSI: 3 to 8 decoder

|  |  |  |
| --- | --- | --- |
|  | A2 A1 A0 | /O0 /O1 /O2 /O3 /O4 /O5 /O6 /O7 |
| 1 0 0 | 0 0 0 | L |
| 0 0 1 | L |
| 0 1 0 | L |
| 0 1 1 | L |
| 1 0 0 | L |
| 1 0 1 | L |
| 1 1 0 | L |
| 1 1 1 | L |
| otherwise | X | H |

A0

A1

A3 74138

/O0-7

E1

/E2

/E3